

*For More Information Contact:*

Bridgid Bartkiewicz  
MEARS Technologies  
617-219-0611  
bridgid.bartkiewicz@mearstechnologies.com

Jessie Hennion  
Porter Novelli  
617-897-8230  
jessie.hennion@porternovelli.com

## **MEARS TECHNOLOGIES CHOSEN TO PRESENT AT SEMICON WEST 2007 TECHNOLOGY INNOVATION SHOWCASE**

*MEARS' MST™ for CMOS Technology Recognized by SEMI Judges for Its Ability to Push the Limits of Moore's Law by Increasing Semiconductor Performance While Reducing Static Power.*

**San Francisco, SEMICON West 2007, Booth T5, July 16, 2007** — MEARS Technologies, Inc., a provider of advanced silicon processes and engineering services to semiconductor device manufacturers and contract foundries, has been selected by SEMI to participate in the Technology Innovation Showcase at SEMICON West 2007, July 16-20, at the Moscone Center in San Francisco, Calif. A SEMI panel of industry judges chose MEARS Technologies as one of 19 companies to present based on the technical merit, commercialization potential and the expected impact the company and its technology will have on the semiconductor and related industries. MEARS Technologies' MST™ for CMOS technology is a new approach to silicon engineering that enables IC makers to simultaneously increase semiconductor performance and reduce static power, while maintaining compatibility with standard manufacturing equipment and processes.

As one of the SEMICON West 2007 Technology Innovation Showcase winners, MEARS Technologies' founder and president, Dr. Robert Mears, will present "MST: A Fab-Friendly Approach for Reducing Gate Leakage," July 17 from 3:30 - 3:50 p.m. at the Device Scaling TechXPOT located in the Moscone Center, North Hall. Launched in 2006, the TechXPOTs are focused "shows-within-the-show" that feature exhibits, special displays and live technical presentations on the latest topics and trends in micro- and nanoelectronics manufacturing, markets and technologies. During SEMICON West, MEARS Technologies also will be available in Technology Innovation Showcase Booth T5 in the North Hall.

MEARS Technologies' MST for CMOS technology is an advanced approach that re-engineers the physical properties of silicon to increase semiconductor power and efficiency and reduce static power at the 65-nm and 45-nm process nodes and beyond. Static power dissipation is a growing problem for chip designers and can account for as much as 60 percent of the power loss in semiconductors manufactured at the 65-nm process node. By enhancing the physical properties of silicon through a breakthrough in quantum engineering, MEARS Technologies' MST for CMOS technology improves overall chip

performance and reduces static power by as much as 80 percent, without introducing new materials into existing manufacturing process flow.

“With each new semiconductor process generation, something challenges the ability of Moore’s Law to continue delivering the performance benefits that the industry has come to expect,” said Dr. Mears.

“Clearly, the issue of transistor static power is one of the most pressing concerns facing IC manufacturers today, particularly at 65 nm, 45 nm and beyond. We’re delighted that SEMI is giving us the opportunity to educate the audience at SEMICON West and explain how MST for CMOS technology can quickly and cost-effectively increase semiconductor performance and efficiency and reduce static power with virtually no impact to the fab line.”

“We are pleased to have MEARS Technologies delivering one of this year’s highly anticipated presentations as a Technology Innovations Showcase winner,” said Ralph Kirk, technical director for SEMI, regarding this year’s SEMICON West show. “As microelectronics take on more characteristics of nanotechnology, it is fitting that companies like MEARS Technologies are tackling the issues of chip performance and power dissipation at the atomic level.”

#### **About MST for CMOS**

Static power dissipation can account for as much as 60 percent of the total power budget of devices manufactured at the 65-nm process node. Using a breakthrough silicon engineering technique, MEARS Technologies has developed its patented MST for CMOS technology to provide a simultaneous increase in transistor performance with dramatically reduced static power, providing a significant advantage for all applications that benefit from reduced power consumption or need to optimize performance per Watt. MEARS Technologies’ MST for CMOS is designed to be fully compatible with semiconductor manufacturers’ baseline processes, whether bulk CMOS, strained silicon, silicon-on-insulator or high-k / metal gate. The improvements are achieved through a band engineering approach that is based on a deep understanding of the quantum mechanics of modern deep-submicron devices. In its first implementation, MST for CMOS is a precision nano-doped silicon layer that is integrated into a standard CMOS flow. The channel replacement layer can be added without introducing new materials in the fabrication process. This “silicon-on-silicon” solution adds only a few steps to the standard CMOS manufacturing flow—at virtually no additional manufacturing cost or yield impact.

#### **About MEARS Technologies**

MEARS Technologies is an emerging materials technology company that provides advanced silicon processes and engineering services to semiconductor device manufacturers and contract foundries. The company combines a core competency in materials engineering and quantum mechanics with practical semiconductor process technology know-how to optimize the power efficiency and performance of

integrated circuits manufactured on deep sub-micron processes. With a licensing model and strong patent position covering breakthrough silicon structures, methods and processes, MEARS Technologies enhances the fundamental electronic properties of silicon without requiring new manufacturing equipment or the use of exotic materials. For more information about MEARS Technologies, please visit [www.mearstechnologies.com](http://www.mearstechnologies.com).

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